

[0027] FIG. 2 is a device typical sectional view corresponding to a section taken along A-A' of a cell area end cutout region R1 of FIG. 1;

[0028] FIG. 3 is a device typical sectional view corresponding to a section taken along line B-B' of a cell area internal cutout region R2 of FIG. 1;

[0029] FIG. 4 is an enlarged top view of a linear unit cell area of FIG. 1 and its peripheral R5 related to a first embodiment (one-dimensional active cell thinned-out structure: corresponding to FIGS. 6 to 8) of the present application;

[0030] FIG. 5 is an enlarged top view of a linear unit cell area of FIG. 1 and its peripheral R5 related to a fifth embodiment (two-dimensional active cell thinned-out structure: corresponding to FIGS. 30 through 32) of the present application;

[0031] FIG. 6 is an overall top view (which approximately corresponds to FIG. 1 but near a more concrete form) of the IE-type trench gate IGBT device chip according to the first embodiment (common even to other embodiments) of the present application;

[0032] FIG. 7 is an enlarged top view (P-type deep floating & hole barrier linear unit cell structure) of a cell area internal cutout region R3 of FIG. 6;

[0033] FIG. 8 is a device sectional view corresponding to a section taken along line D-D' of FIG. 7;

[0034] FIG. 9 is a device sectional view in a manufacturing process (hole barrier region introduction step) corresponding to FIG. 8 for describing a manufacturing method corresponding to a device structure of the first embodiment of the present application;

[0035] FIG. 10 is a device sectional view in the manufacturing process (P-type floating region introduction step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0036] FIG. 11 is a device sectional view in the manufacturing process (trench processing hardmask deposition step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0037] FIG. 12 is a device sectional view in the manufacturing process (trench hardmask processing step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0038] FIG. 13 is a device sectional view in the manufacturing process (trench hardmask processing resist removal step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0039] FIG. 14 is a device sectional view in the manufacturing process (trench processing step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0040] FIG. 15 is a device sectional view in the manufacturing process (trench processing hardmask removal step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0041] FIG. 16 is a device sectional view in the manufacturing process (extension diffusion and gate oxidizing step) corresponding to FIG. 8 for describing the manufacturing

method corresponding to the device structure of the first embodiment of the present application;

[0042] FIG. 17 is a device sectional view in the manufacturing process (gate polysilicon deposition step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0043] FIG. 18 is a device sectional view in the manufacturing process (gate polysilicon etchback step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0044] FIG. 19 is a device sectional view in the manufacturing process (gate oxide film etchback step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0045] FIG. 20 is a device sectional view in the manufacturing process (P-type body region and N+ type emitter region introduction step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0046] FIG. 21 is a device sectional view in the manufacturing process (interlayer insulating film deposition step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0047] FIG. 22 is a device sectional view in the manufacturing process (contact hole formation step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0048] FIG. 23 is a device sectional view in the manufacturing process (substrate etching step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0049] FIG. 24 is a device sectional view in the manufacturing process (P+ type body contact region and P+ type latchup prevention region introduction step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0050] FIG. 25 is a device sectional view in the manufacturing process (surface metal deposition step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0051] FIG. 26 is a device sectional view in the manufacturing process (backgrinding and back surface impurity introduction step) corresponding to FIG. 8 for describing the manufacturing method corresponding to the device structure of the first embodiment of the present application;

[0052] FIG. 27 is a device sectional view corresponding to a section taken along line D-D' of FIG. 7 for describing a device structure of an IE-type trench gate IGBT according to a second embodiment (P-type deep floating structure) of the present application;

[0053] FIG. 28 is a device sectional view corresponding to a section taken along line D-D' of FIG. 7 for describing a device structure of an IE-type trench gate IGBT according to a third embodiment (P/N-type floating & hole barrier structure) of the present application;